level, while operating to relatively high I/O voltages, close to—or exceeding—the level where the lifetime of the device is reduced by the effects of hot-carrier induced gate degradation.

[0011] Some alternatives have been previously discussed in the literature in order to overcome the gate reliability problem in the protection devices without degradation of the device's ESD performance. Solutions in prior art consider devices with a floating gate, sometimes referred to as devices with a dummy gate. However, these devices are highly dependent on the rise time and decay time of the ESD event as well as on temperature fluctuations. Results show that different versions of devices with floating gates exhibit characteristics that may cause a misleading interpretation of the device performance.

[0012] In a floating gate device, the conduction characteristics are unpredictably modified by the gate conditions. For instance, during an ESD event the gate MOS capacitor can become charged as a result of the ESD event. Since the gate voltage is not controlled, the charges underneath the gate are not immediately depleted back to the initial conditions and consequently the protection device can stay in the on-state. The leakage current through the channel of the protection device increases abruptly, leading to a circuit latchup, failure of the ESD protection, and/or further damage of the protected IC.

[0013] Thus, there is a need to overcome these and other problems of the prior art to obtain a protection device without gate reliability problems. Moreover, there is a need for sub-micron CMOS technology to be able to pass a high level of ESD current without latchup or damage. Further, there is a need for a device that can operate and protect against ESD during extreme temperature conditions, variable pulse rise times and pulse widths, and that is reliable during very extreme operating conditions.

SUMMARY OF THE INVENTION

[0014] In accordance with the present teachings, there is a substrate triggered thyristor (STT) with tunable trigger and holding voltages fabricated in complementary n- and p-types using a sub-micron CMOS technology. The STT is utilized for designing input/output (I/O) pad ESD protection and ESD supply clamps that are immune to latchup. The trigger and holding voltages of this device can be adjustable to protect both CMOS standard digital circuits and ICs with bipolar I/O signals higher than and lower than the core circuit power supplies. The measured TLP (transmission line pulse) current-voltage (I-V) characteristics demonstrate trigger voltages tunable in the range of 10 V to 20 V, holding voltage tunable in the range of 1.9 V to 16V, adjustable holding current, and low on-state resistance.

[0015] In accordance with the present teachings, there is a tunable thyristor device without a gate for the design of ESD protection at I/O pads and as a supply clamp for CMOS circuits. The device is designed using two different structures and also has complementary versions, n- and p-type. The disclosed protection device will be referred to hereinafter as a substrate triggered thyristor (STT). This device can be classified in two types: 1) n- and p-type double-substrate-triggered thyristor (n- and p-type DSTT) and 2) n- and p-type single-substrate-triggered-thyristor (n- and p-type SSTT). The present teachings provide a versatile, space-efficient, and reliable ESD protection device for a more robust implementation of ESD protection systems in advanced sub-micron CMOS technologies.

[0016] The n- and p-type STT devices can be fabricated using a standard sub-micron CMOS process. The spacing and dimensions of the doped regions of n- and p-type STTs can be adjusted to obtain different current-voltage (I-V) characteristics. The disclosed STTs can protect a core circuit in a broad range of applications including: 1) ICs where the I/O signal swings within the range of the core circuit power supplies, for example, a standard digital microchip, and 2) ICs where the I/O signal is bipolar and below/above the range of the core circuit power supplies, for example, communication transceivers included in personal computers, industrial applications, and as standard equipment for local area networks (LANs) and closed circuit security systems.

[0017] According to various embodiments, an electrostatic discharge (ESD) device is provided. The ESD device can comprise a substrate doped to a first conductivity type and a first well doped to the first conductivity type disposed in the substrate. The first well can comprise a first region doped to the first conductivity type, a second region doped to a second conductivity type, and a first isolation region disposed between the first region and the second region. The ESD device can also comprise a second well doped to a second conductivity type disposed in the substrate adjacent to the first well, where the second well can comprise a third region doped to the first conductivity type, a fourth region doped to the second conductivity type, and a second isolation region disposed between the third region and the fourth region. Still further, the ESD device can include a first trigger contact comprising a highly doped region disposed at a junction between the first well and the second well.

[0018] According to various embodiments, another electrostatic discharge (ESD) device is provided. The ESD device can comprise a substrate doped to a first conductivity type and an epitaxial layer formed in the substrate and doped to a second conductivity type. A first well can be disposed in the substrate and doped to the first conductivity type, the first well comprising a cathode comprising a first region doped to the first conductivity type and a second region doped to the second conductivity type and separated from the first region by a first isolation region. A second well can be disposed adjacent to the first well and doped to the second conductivity type, the second well comprising an anode comprising a third region doped to the first conductivity type. The ESD device can further include a first trigger contact having a length D**1** disposed at a junction between the first well and the second well and between a second isolation region and a third isolation region.

[0019] According to various embodiments, a method of making an electrostatic discharge (ESD) device is provided. The method can comprise providing a substrate doped to a first conductivity type and forming a first well doped to the first conductivity type in the substrate. The first well can comprise a first region doped to the first conductivity type a second region doped to a second conductivity type, and a first isolation region disposed between the first region and the second region. The method can further comprise forming a second well doped to a second conductivity type in the substrate adjacent to the first well, the second well compris-